50% PAE WCDMA Basestation Amplifier Implemented with GaN HFETs

Don Kimball, Paul Draxler, Jinho Jeong, Chin Hsia, Sandro Lanfranco, Walter Nagy, Kevin Linthicum, Larry Larson and Peter Asbeck

***Abstract*—A high performance GaN HFET WCDMA basestation power amplifier is presented, which uses an envelope tracking bias system to achieve high linearity and efficiency. The measured overall power-added efficiency (PAE) reached 50.7 %, with a normalized power RMS error of 0.7% and ACLR of -52 dBc at an offset frequency of 5 MHz, at an average output power of 37.2 W and gain of 10.0 dB for a single carrier WCDMA signal. To the authors' knowledge, this corresponds to the best efficiency reported for a single stage base station power amplifier. Digital predistortion (DPD) was used at two levels: memoryless DPD to compensate for the expected gain variation of the amplifier over the bias envelope trajectory, and deterministic memory mitigation, to further improve the linearity. The signal envelope had a peak-to-average power ratio of 7.67 dB.**

***Index Terms*— Base station power amplifier, efficiency, envelope tracking, digital predistortion, WCDMA, GaN HFET.**

I. Introduction

High power-added efficiency is an important objective for base-station amplifiers, influencing thermal management, reliability, and cost. It is challenging to maintain high efficiency during operation over the wide instantaneous power range required for modern communication signals such as WCDMA, while maintaining tight error vector magnitude (EVM) and ACLR specifications. Si LDMOS has been a popular transistor choice for base station high power amplifiers, since LDMOS technology can provide reliable and cost effective solutions [1]. However, in order to obtain better linearity and efficiency for 3G wireless base stations, intense research on high voltage GaAs HBTs[2] and FETs[3], and GaN HFETs[4][5] has been carried out. GaN HFETs are attractive options since they can provide higher voltage and higher power density than the other high power devices.

Recently, high performance GaN HFETs on Si substrates (instead of the more customary sapphire or silicon carbide substrates) have been reported showing 150 W output power for WCDMA base stations [5]. In this work, GaN HFETs on Si substrates were used in a WCDMA base station amplifier, in which high efficiency was achieved by using an envelope tracking technique on the drain bias. The envelope tracking architecture employs a dynamic supply voltage that tracks the input RF envelope for efficiency enhancement. In the system, shown schematically in Fig. 1, the dynamic supply voltage is provided by a high efficiency wideband envelope amplifier. Measurements reported here show that the overall system exceeds the linearity requirements for WCDMA and achieves record overall efficiency (accounting for power dissipated by both the RF amplifier and the envelope amplifier). The efficiency attained in the envelope tracking amplifier is dramatically better than that obtained with constant drain voltage, because 1) the amplifier operates closer to saturation, 2) the transistor temperature is maintained at a lower value, and 3) the dynamic peak voltage reaches higher values than can be used for constant drain bias voltages.

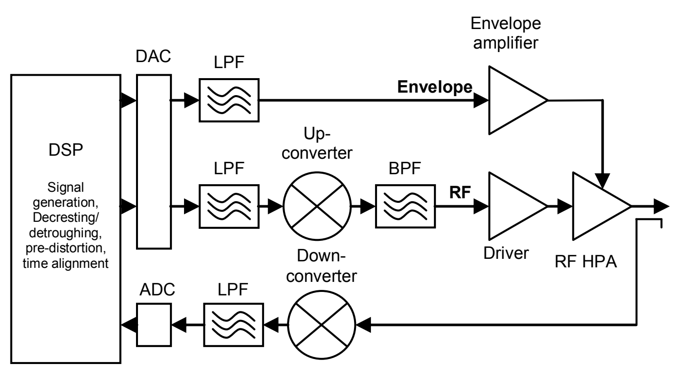

Figure. 1. Block diagram of envelope tracking base-station amplifier

II. GaN HFET-BASED RF AMPLIFIER

GaN HFETs employed in this work are based on epitaxial layers grown by MOCVD on 100 mm floatzone silicon (111) substrates. The growth process was nucleated with AlN, followed by a transition layer of AlGaN, a 0.8um unintentionally doped GaN buffer layer, an AlGaN barrier layer and a capping layer. A SiN film was used to passivate the surface. Isolation was achieved via multiple energy N+ implantation. The gate length was 0.7um, and the overall gate width of the HFETs was 36 mm, composed of 180 fingers of

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200um unit width. Via contacts through the substrate (Si wafers with resistivity greater than 10,000 ohm cm) were employed to contact the sources.

The packaged device (Nitronex NPT 21120) consists of two HFETs combined in a CuW / ceramic package (to provide an aggregate gate width of 72mm). Internal matching circuits to provide an impedance 3-j4 ohm at 2.14 GHz for both the input and output of the FET were also provided in the package. The FET was biased in class AB mode. Impedance matching via microstrip lines and shunt capacitors was used on input and output as shown in Fig 2. No harmonic terminations were explicitly provided. The implemented RF power amplifier shows a 150 W peak under CW operation at 2.14 GHz. The measured drain efficiency with fixed drain bias of 28 V and quiescent current of 2400 mA reached 25 % at -39 dBc ACLR under WCDMA signal (test model 1 with 64 users, peak-to-average power ratio of 8.5 dB at 0.1 % probability and 9.8 dB at 0.01 %). The corresponding output power was 19 W and the gain was 15.0 dB at the center frequency of 2.14 GHz [5].

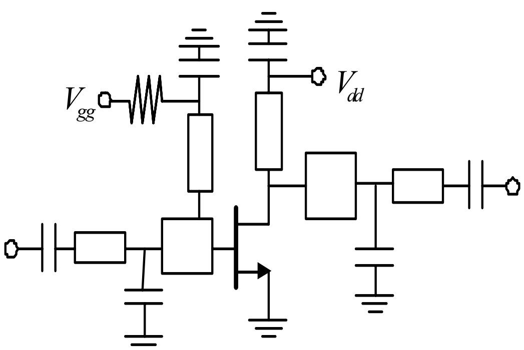

Figure 2: Circuit diagram of Class AB RF amplifier output stage.

III. WIDEBAND HIGH EFFICIENCY ENVELOPE AMPLIFIER

The envelope amplifier used in this work, shown schematically in Fig. 3, comprises a linear stage to provide a wideband voltage source and, in parallel, a switching stage to provide an efficient current supply. The output voltage of the envelope amplifier follows the input envelope signal with help of an operational amplifier. The current is supplied to the RF amplifier drain from both the linear stage and the switching stage through a current feedback network which senses the current flowing out of the linear stages and turns on/off the switch [7]. The linear stage provides the difference between the desired output current and the current provided by the switching stage, such that the overall error is minimized.

Measurement of the high voltage envelope amplifier used in this work shows efficiency of approximately 77 % under WCDMA signals. At full output power, the peak output voltage was 29.5 V and the RMS(root-mean-square) voltage was 13.8 V.

IV. PREDISTORTION SYSTEM

The WCDMA signal is generated in the digital domain, and consists of an envelope signal, as well as I and Q RF signals. After up-conversion, the resultant RF signal provides the input to the RF amplifier, whose supply voltage is modulated by the amplified envelope signal by the wide band and high efficiency envelope amplifier. To minimize distortion by the time delay difference between the Vdd envelope and RF path, synchronization is performed by comparing the input and down-converted output signal [6]. A memoryless pre-distortion (DPD) is also carried out in the digital domain in order to minimize the AM-AM and AM-PM distortion caused by the RF amplifier and envelope amplifier. Decresting (an adjustment of the peak-to-average ratio), is performed digitally on the envelope of the signal to optimize the efficiency, ACLR and EVM performance. To avoid gain collapse of the RF amplifier at low drain voltages, the envelope of the signal is also detroughed (adjustment is made to the envelope signal in the vicinity of its zeros). A second level memory mitigation DPD is performed that compensates for a perturbation to the instantaneous gain caused by deterministic memory effects [8].

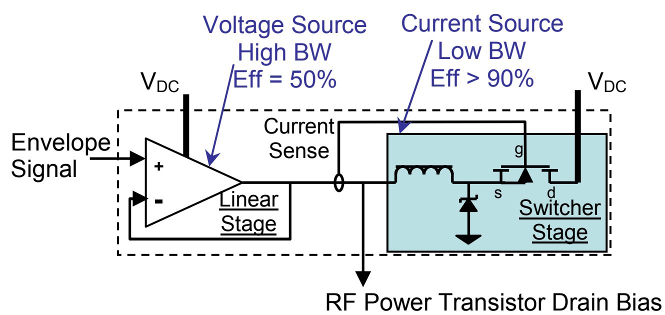

Figure. 3: Schematic diagram of high efficiency envelope amplifier.

V. MEASUREMENT RESULTS

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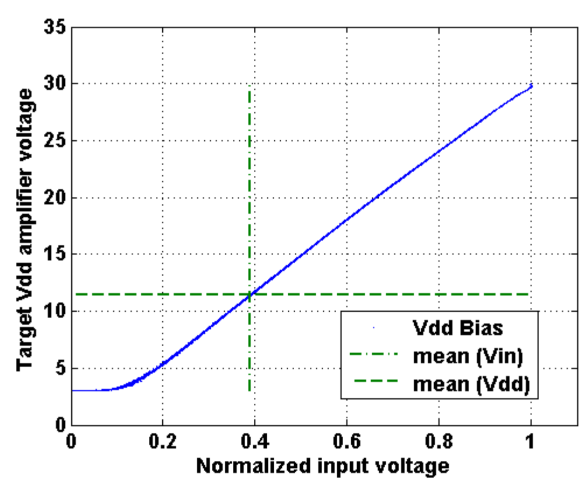
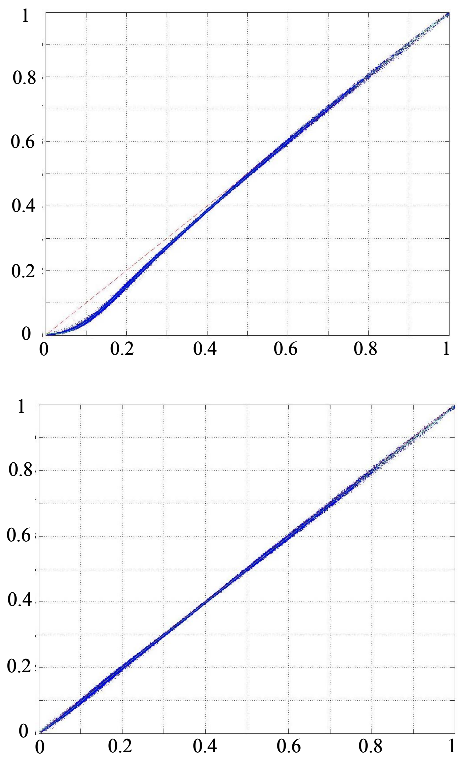
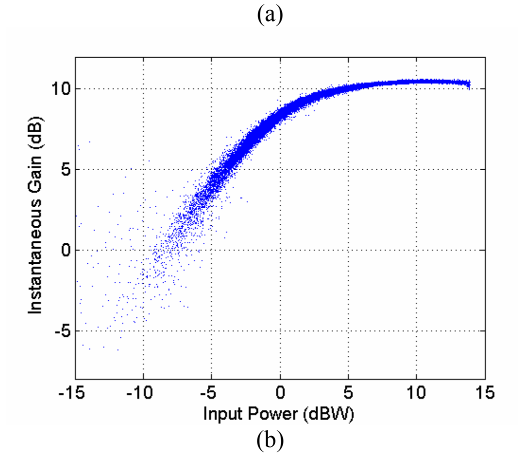


Figure 5. Vdd target voltage for the normalized input voltage.

an output power which also tracks the drain voltage (Fig. 6). The overall improvement in output signal quality is quite apparent from the measured output spectrum as shown in Fig. 7, where ACLR is improved by 15.0 dB and 12.0 dB at 5 MHz offset and 10 MHz offset, respectively, through the digital pre-distortion. The ACLR specification limits for WCDMA radio basestation output signals are -45 dBc at the 5 MHz offset and -50 dBc at the 10 MHz offset, so the specifications are met with adequate margin.



(a)



(b)

Figure 4. (a) Measured AM-AM performance (y-axis : normalized output amplitude, x-axis : normalized input amplitude on a linear scale). Left figure : before pre-distortion, right figure : after pre-distortion. (b) with a more traditional log scale: Gain(db), Pin(dBW). Note, the value of Vdd is swept along with the instantaneous input power.

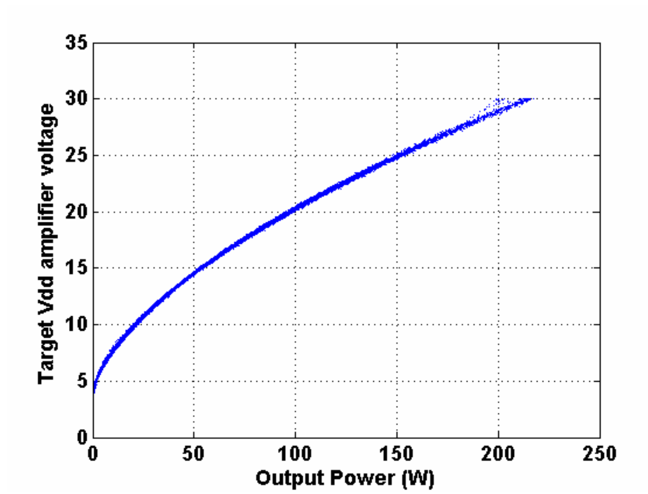


Figure 6. Vdd target voltage over measured output power.

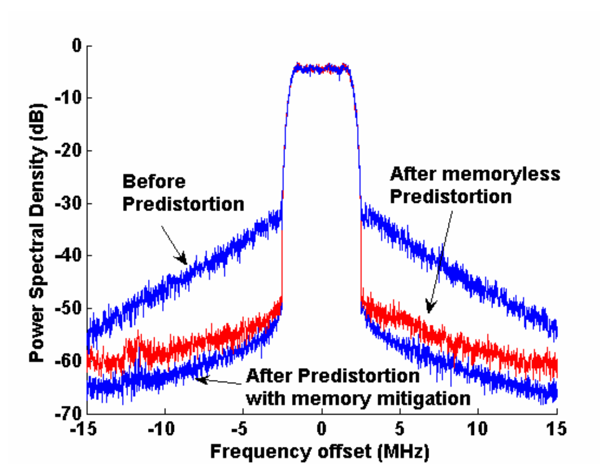


Figure. 7. Normalized output power spectral density before and after pre-distortion of a single carrier WCDMA signal

Even with the outstanding performance of the memoryless DPD, we applied a memory mitigation algorithm [8] to evaluate the memory effects associated with this device. The improvement of output RMS error with iteration count of the algorithm is presented in Fig. 8.

The average power added efficiency (PAE) including dissipation in the envelope amplifier is as high as 50.7 % with average output power of 37.2 W. This is the highest efficiency among the reported WCDMA base station power amplifiers. The gain and error vector magnitude (EVM) are 10.0 dB and 1.74 % after memoryless pre-distortion, respectively. After memory mitigation, the measured EVM drops to 0.7% and ACLR to -52.0 dBc at 5 MHz offset and -58.0 dBc at 10 MHz offset. Table 1 summarizes the measured performance of the amplifier with a single carrier WCDMA signal.

VI. Summary and Conclusions

In this paper, a WCDMA base station power amplifier using GaN HFETs on Si substrates and envelope tracking was presented, demonstrating very high efficiency and precise output performance. Under the influence of a WCDMA source, an average efficiency of 50.7 % with average output power of 37.2 W and gain of 10.0 dB was achieved with an output EVM of 0.7%. The results illustrate the potential of GaN HFETs, in combination with advanced amplifier architectures, to achieve dramatic improvements in basestation power amplifiers.

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Table 1. Summarized performance of power amplifier with single carrier WCDMA signal and digital predistortion

	Gain (dB)	Po (W)	DE (%)	PAE (%)	EVM (%)	ACLR1 (dBc)	ACLR2 (dBc)
Before	10.3	36.5	51.7	49.3	12.1	-32	-41
After ML DPD	10	37.2	53.4	50.7	1.74	-48	-53
After Memory DPD	-	-	-	-	0.7	-52	-58

DE : drain efficiency.
ML DPD: Memoryless digital predistortion
Spedification requirements: ACLR1 < -45 dBc, ACLR2 < -50 dBc.
ACLR1 and ACLR2 : ACLR at 5 and 10 MHz offset, respectively.
Gain, Po, DE, and PAE didn't change significantly between After ML DPD and After Memory DPD.

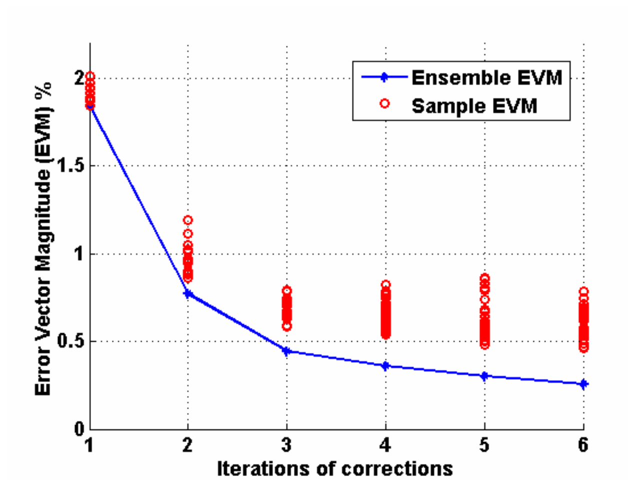

Figure. 8. WCDMA signal EVM improvements over memory effect mitigation iterations for single sequences and ensample averages.